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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/488,313	01/20/2000	James E. Tatem JR.	47571-P012US-09904363	4257

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EXAMINER
WILLIAMS, DEMETRIA A

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/488,313	TATEM, JAMES E.	
	Examiner	Art Unit	
	Demetria A. Williams	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,9,10,12-14,16-20,22-25,34,35,45,48-50,53-55 and 61* is/are rejected.

7)☒ Claim(s) *2,5-8,11,15,21,26-33,36-44,46,47,51,52, and 56-60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 12-14, 16, 17, 23, 24, 34, and 35 rejected under 35 U.S.C. 102(e) as being anticipated by Yang.

3. Regarding claim 1, Yang discloses a system and method for automatic frequency control comprising a controllable oscillator, a phase lock loop (PLL) coupled to the oscillator, and a control circuit for adjusting the operating range of the oscillator to a range capable of operating the PLL (see generally column 3, lines 35-53; column 1, lines 34-40).

4. Regarding claim 12, Yang further discloses storage for storing the frequency change value, which is a form of memory (see generally column 3, lines 50-53).

5. Regarding claims 13 and 14, Yang discloses that the voltage of the controllable oscillator that is in the range capable of operating the PLL is stored (see generally column 3, lines 50-53).

6. Regarding claim 16, Yang further discloses an algorithm for selecting the appropriate operating range for which to adjust the oscillator in order to synchronize with the PLL (see generally column 3, lines 49-53).

7. Regarding claim 17, Yang discloses that the adjustment is made in order to acquire synchronization by increasing or decreasing the frequency. Since the applicant defines no measure of efficiency and since Yang's goal is to achieve frequency synchronization, the method is considered efficient.

8. Regarding claim 23, Yang further discloses a signal comparison means for providing control information based on this comparison, which would include information regarding a match or lack thereof (see generally column 2, lines 55-67).

9. Regarding claim 24, Yang discloses a method for synchronization comprising operating a controllable oscillator in a PLL mode when the oscillator is operating within range of the PLL, which inherently contains an oscillator, detecting when the synchronization cannot be maintained and operating in a sweep mode when the oscillator is unable to remain synchronized to the PLL (see generally column 3, lines 29-67). The sweep mode provides control signals to adjust the operating range of the oscillator and detecting if the when the PLL mode is able to acquire synchronization, repeating the process as needed (see generally column 3, lines 44-55).

10. Regarding claims 34 and 35, Yang further discloses monitoring the control information used to adjust the oscillator and storing the value used to make the adjustment (see generally column 3, lines 44-53).

11. Claims 53 and 61 are rejected under 35 U.S.C. 102(e) as being anticipated by Tomesen et al ("Tomesen").

12. Regarding claim 53, Tomesen discloses a method of frequency compensation comprising providing a PLL mod of operation to maintain frequency lock, providing a sweep mode to step operation of PLL over a range of frequencies, and monitoring the sweep mode to determine the range of frequencies able to successfully maintain frequency lock (see generally column 5, lines 55-67). Tomesen further discloses that the steps are used to compensate for frequency drift (see abstract).

13. Regarding claim 61, Tomesen further discloses storing information regarding the optimum lock position (see generally column 5, lines 55-59).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Bogdan.

16. Regarding claim 3, Yang discloses all of the elements as described above in reference to claim 1, but does not specify the use of a digital phase lock loop (DPLL). Bogdan discloses a frequency control system comprising a DPLL, which generally requires the use of a digital-to-

analog converter (DAC) (see generally column 2, lines 4-16). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Yang to include the use of a DPLL and DAC, as disclosed by Bogdan because the DPLL alleviates problems such as drift sensitivity (see generally column 2, lines 7-8).

17. Regarding claim 9, Yang further discloses a buffer storage means for storing the frequency control value (see generally column 3, lines 50-53).

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Bogdan as applied to claim 3, and further in view of Adams et al ("Adams"). Yang and Bogdan disclose all of the elements as described above in reference to claim 2, however, neither specify a type of DAC to be used. Adams teaches that sigma-delta DACs, which are high resolution DACs, provide many benefits over the traditional DAC such as less distortion and aliasing (column 2, lines 42-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a high resolution DAC, such as a sigma-delta converter, in order to decrease signal distortion and aliasing.

19. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Bogdan as applied to claim 9 above, and further in view of Shohara. While Yang and Bogdan disclose all of the elements as applied above, neither include the use of hysteresis control. Shohara discloses an automatic frequency control system wherein changes are made to the controllable oscillator frequency only when the offset exceeds a predetermined value (see generally column 18, line 56 – column 19, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Yang to include

changing the oscillator frequency based on a hysteresis value as described by Shohara in order to prevent unnecessary changes which can introduce errors.

20. Claims 18-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Tomesen. Yang discloses all of the elements as applied above to claim 17 but does not specifically recite that the scan is performed on a contiguous portion of the frequency range. Tomesen discloses a system for frequency control wherein a nominal frequency value is used as a starting point for sweeping around a particular set of frequencies with a certain step size (column 5, lines 55-65; column 7, lines 53-63). This includes positions both above and below the nominal position. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Yang to include scanning a contiguous portion of the frequency range around a nominal value in order to quickly acquire synchronization by focusing on those values closest to the expected value.

21. Regarding claim 20, Tomesen further discloses that when an optimum lock position is found, this point is stored in memory (column 5, lines 57-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the frequency towards this direction since it allowed for frequency synchronization.

22. Regarding claim 22, Yang discloses all of the elements as described above in reference to claim 1. While Yang does not specify that the operating range is selected to accommodate frequency drift associated with the life of the system, such a drift is well known in the art. Further, Tomesen discloses that tuning is used to compensate for frequency drift.

23. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Adams and Bogdan. Yang discloses all of the elements as described above in reference to claim 24, but does not disclose the use of a digital PLL or high resolution DAC. Bogdan discloses a frequency control system comprising a DPLL, which generally requires the use of a digital-to-analog converter (DAC) (see generally column 2, lines 4-16). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Yang to include the use of a DPLL and DAC, as disclosed by Bogdan because the DPLL alleviates problems such as drift sensitivity (see generally column 2, lines 7-8). Further, Adams teaches that sigma-delta DACs, which are high resolution DACs, provide many benefits over the traditional DAC such as less distortion and aliasing (column 2, lines 42-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a high resolution DAC, such as a sigma-delta converter, in order to decrease signal distortion and aliasing.

24. Claim 45 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui in view of Bogdan and Adams. Fukui discloses a system for automatic frequency compensation comprising a voltage controlled oscillator (figure 1, reference character 10), a digital-to-analog converter (DAC) (figure 1, reference character 90), a phase locked loop (PLL) for controlling the oscillator (figure 1, reference character 20), and control circuitry for providing control bits to the DAC for adjusting the oscillator when it is not in the operating range of the PLL (figure 1, reference characters 60, 70, and 100). See also column 1, lines 13-40 and column 4, lines 1-40.

Fukui does not specify that the DAC is of high resolution or that the PLL is a digital PLL. However, as Adams points out, the benefits of using a high-resolution converter are well known in the art such as less distortion and aliasing (column 2, lines 42-45). Further, Bogdan points out that the use of a digital PLL reduces drift sensitivity (column 2, lines 4-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Fukui to include the use of a digital PLL and high resolution DAC, as described by Adams and Bogdan, in order to reduce distortion and drift sensitivity.

25. Regarding claim 48, Fukui further discloses that the arithmetic-processing unit monitors the voltage-controlled oscillator (see generally column 2, lines 11-34; column 4, lines 15-37).

26. Regarding claim 49, Fukui further discloses storing the control information in the arithmetic processing unit or outside of the unit (see generally column 4, lines 26-30).

27. Regarding claim 50, Fukui further discloses determining the point at which the desired level of frequency compensation is achieved and storing this information which is then sent to the DAC for controlling the oscillator (see generally column 4, lines 15-37).

28. Claims 54 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomesen. Tomesen discloses all of the elements as described above in reference to claim 53. While Tomesen does not specify that different control signals are used with the different modes of operation, this would have been obvious to one of ordinary skill in the art at the time of the invention because different signals would be required in order to distinguish between the modes. Regarding claim 55, Tomesen further discloses that the oscillator is a voltage-controlled oscillator (see generally column 6, lines 53-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetria A. Williams whose telephone number is (703) 305-4078. The examiner can normally be reached on Monday - Friday, 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

daw
February 24, 2003